

1774

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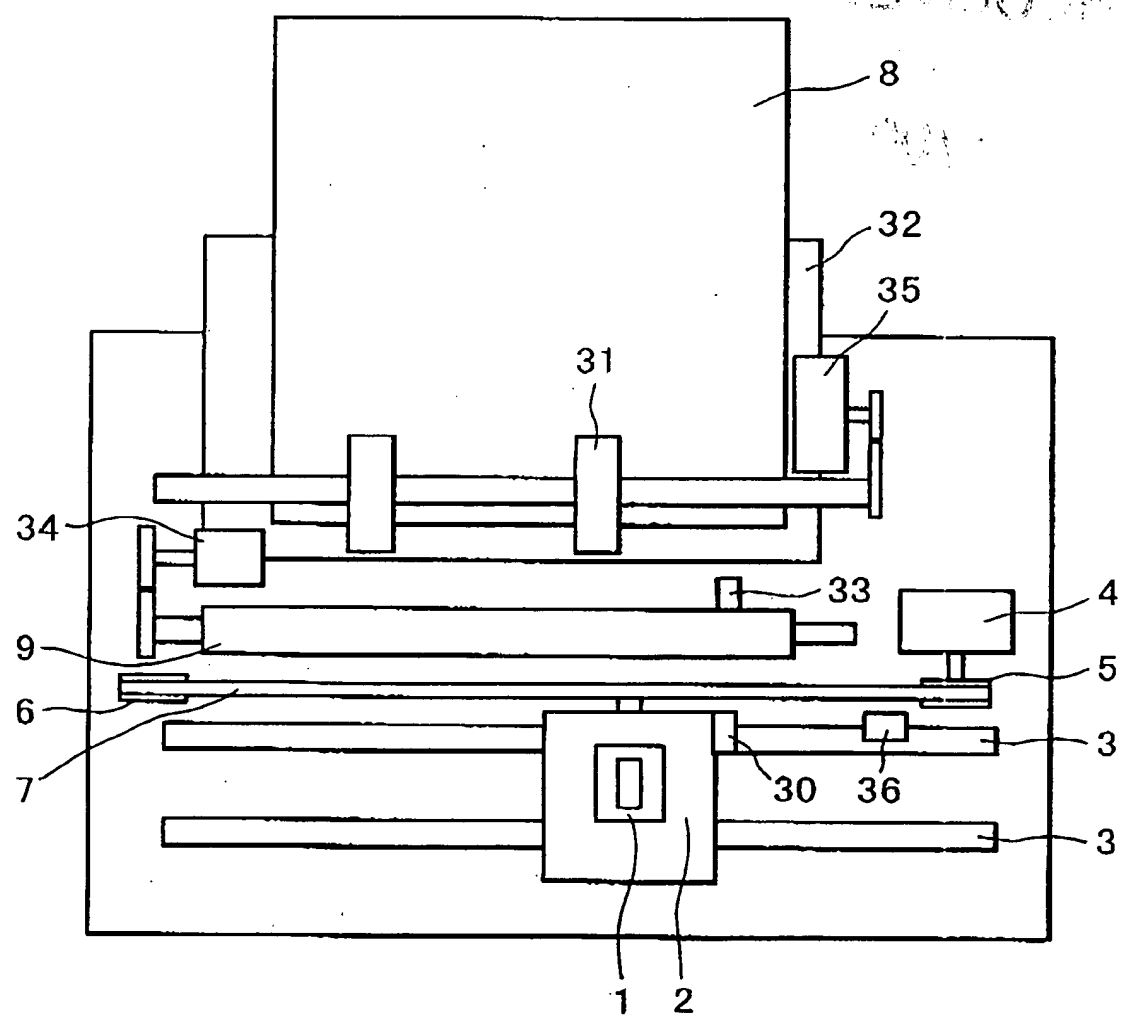


FIG. 1

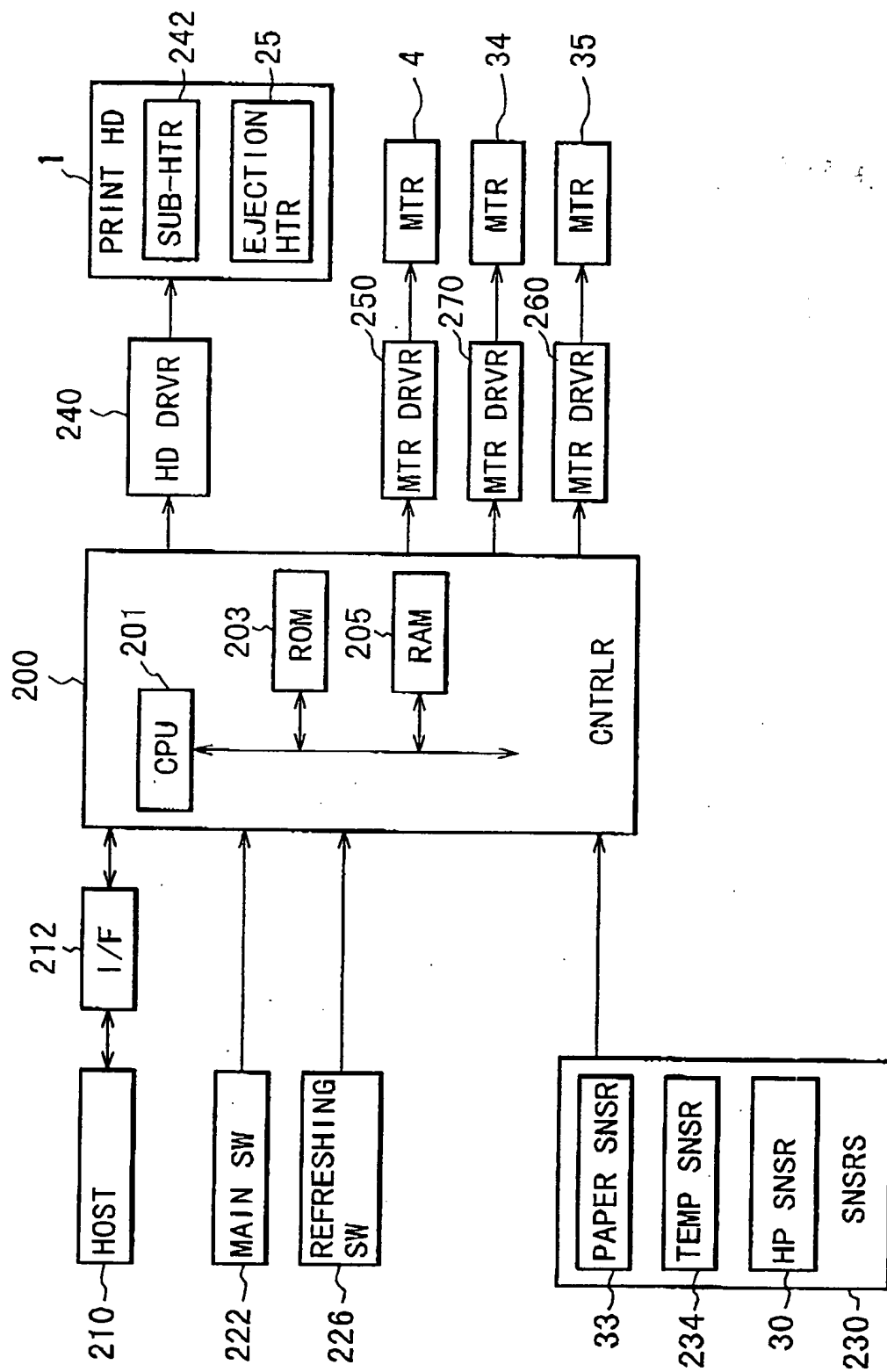


FIG. 2

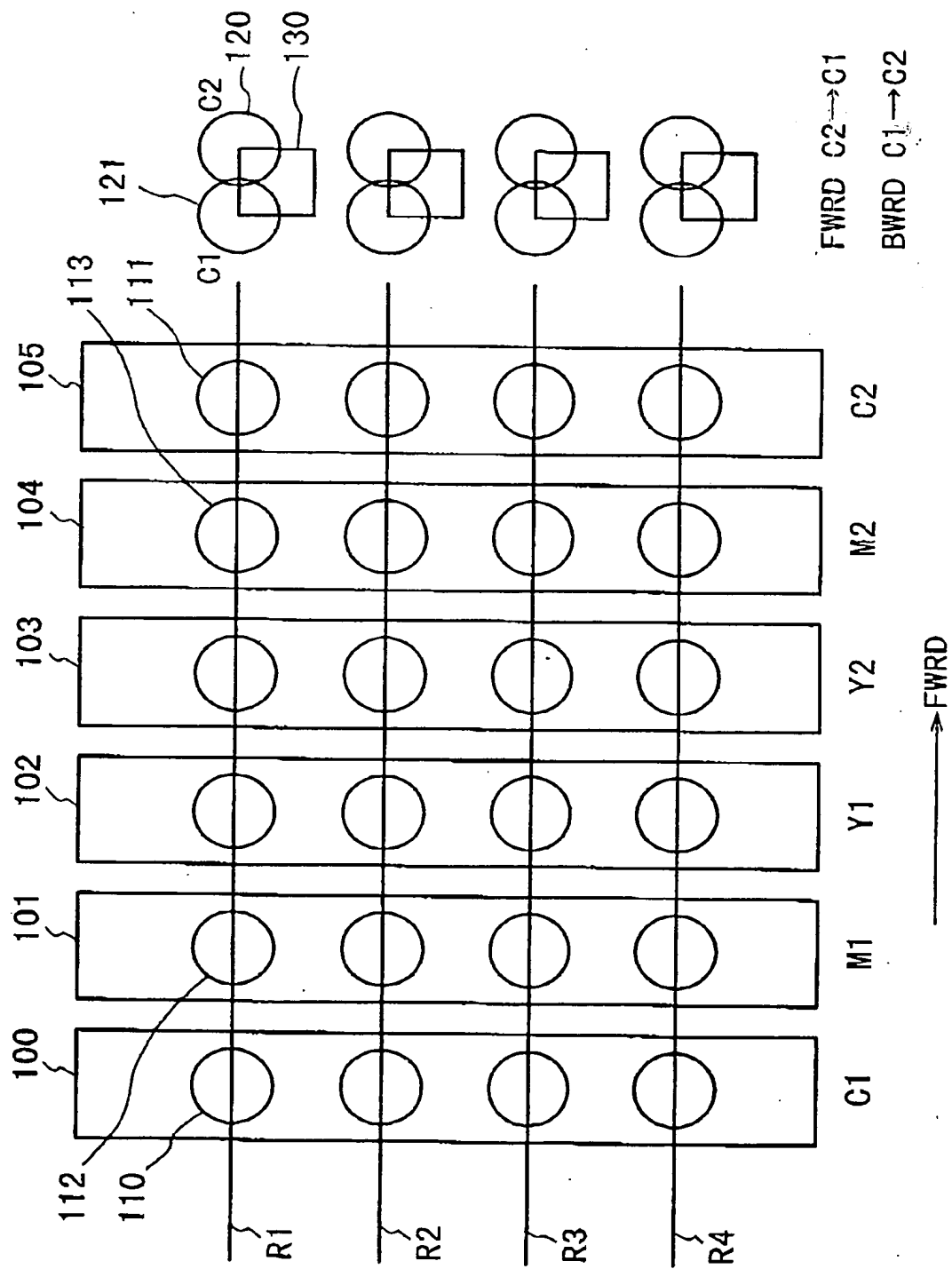


FIG. 3

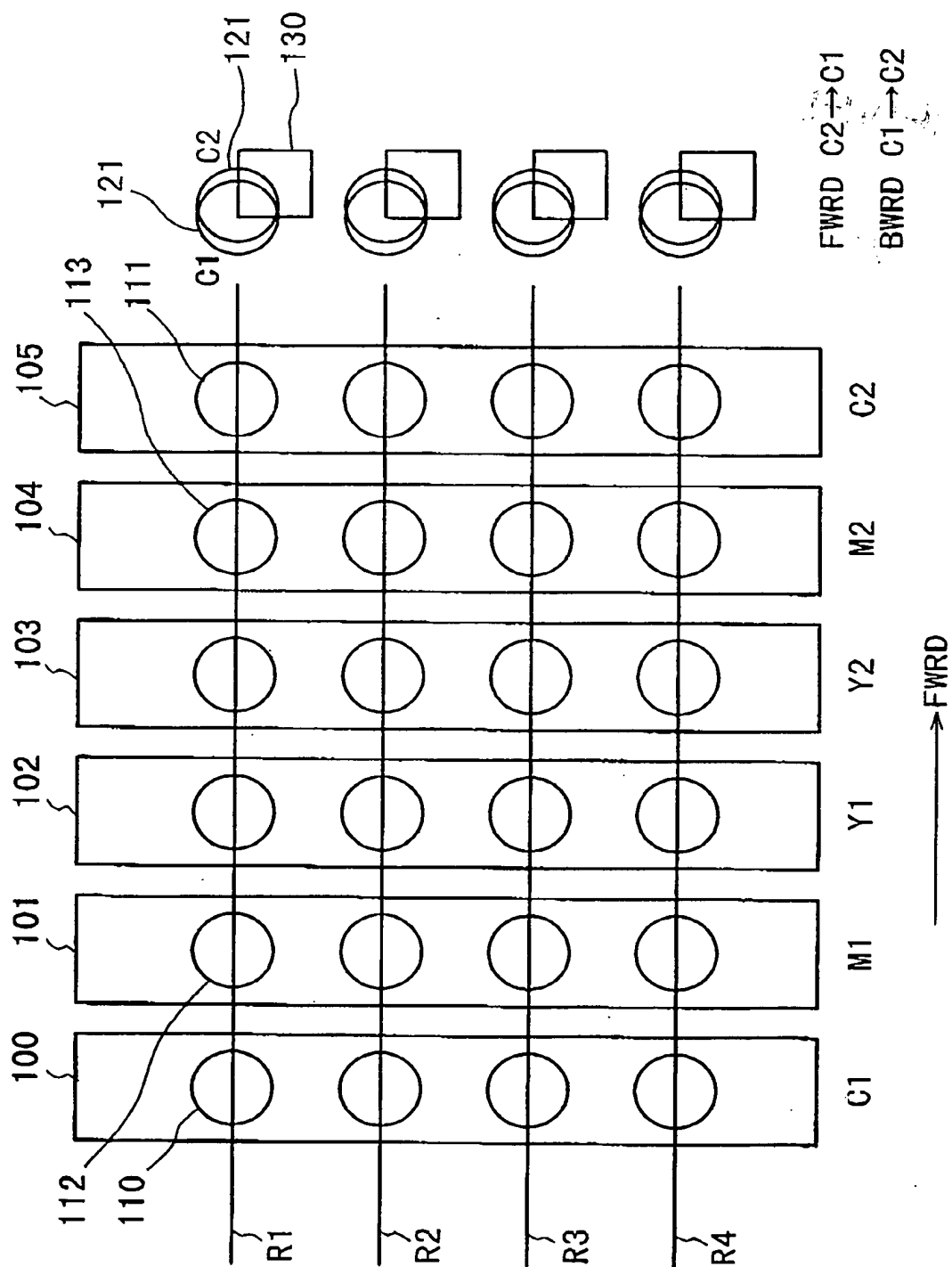


FIG. 4

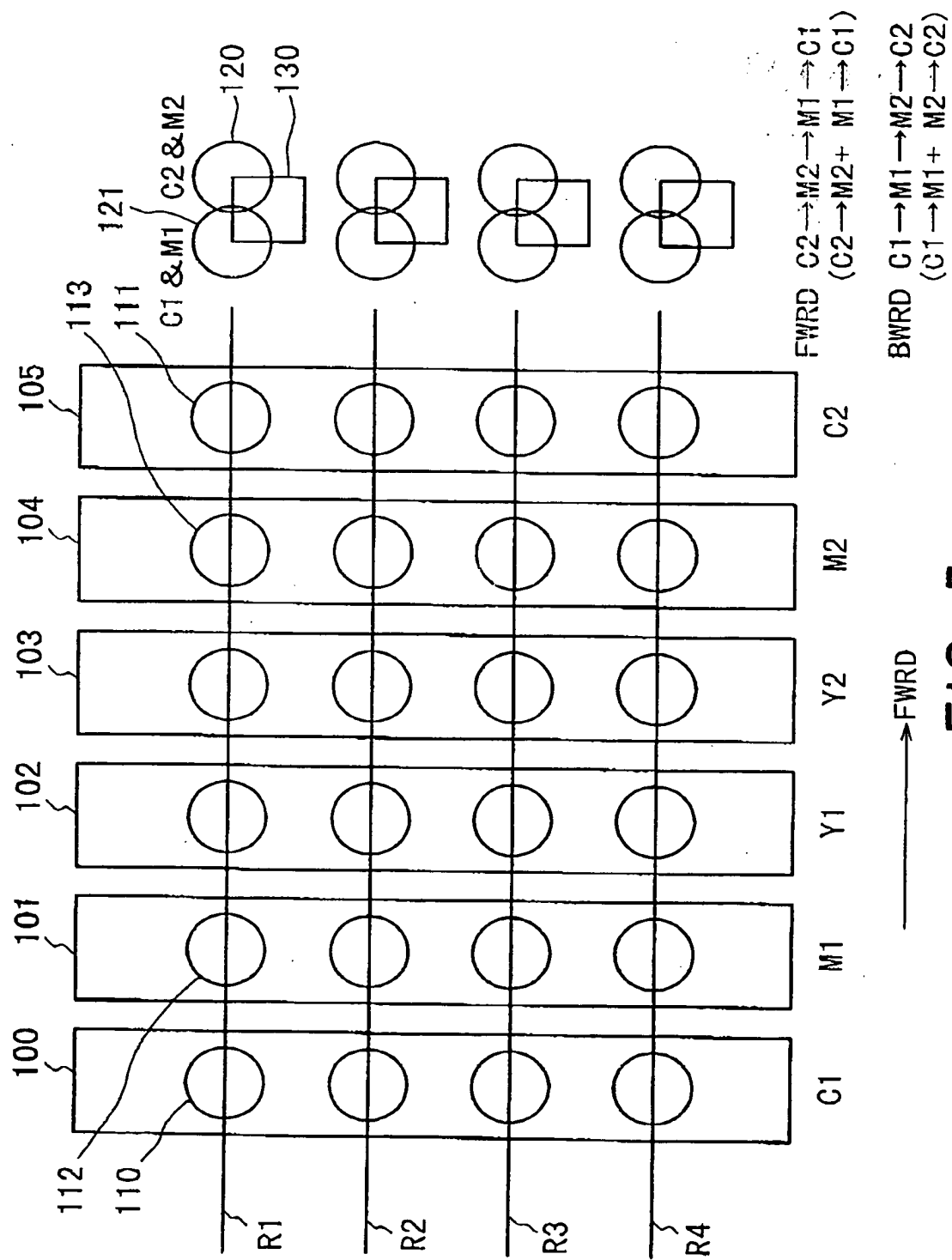


FIG. 5

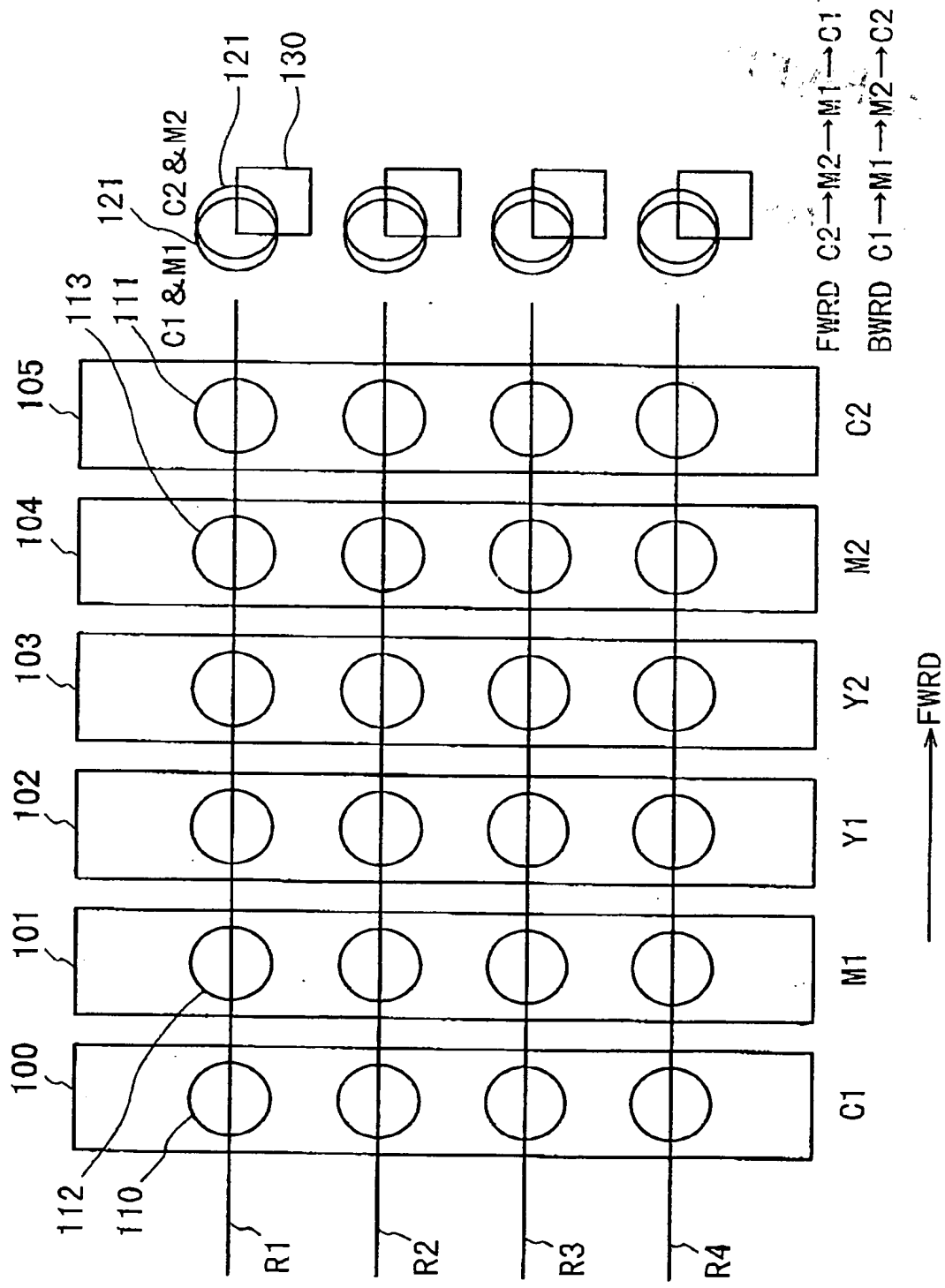


FIG. 6

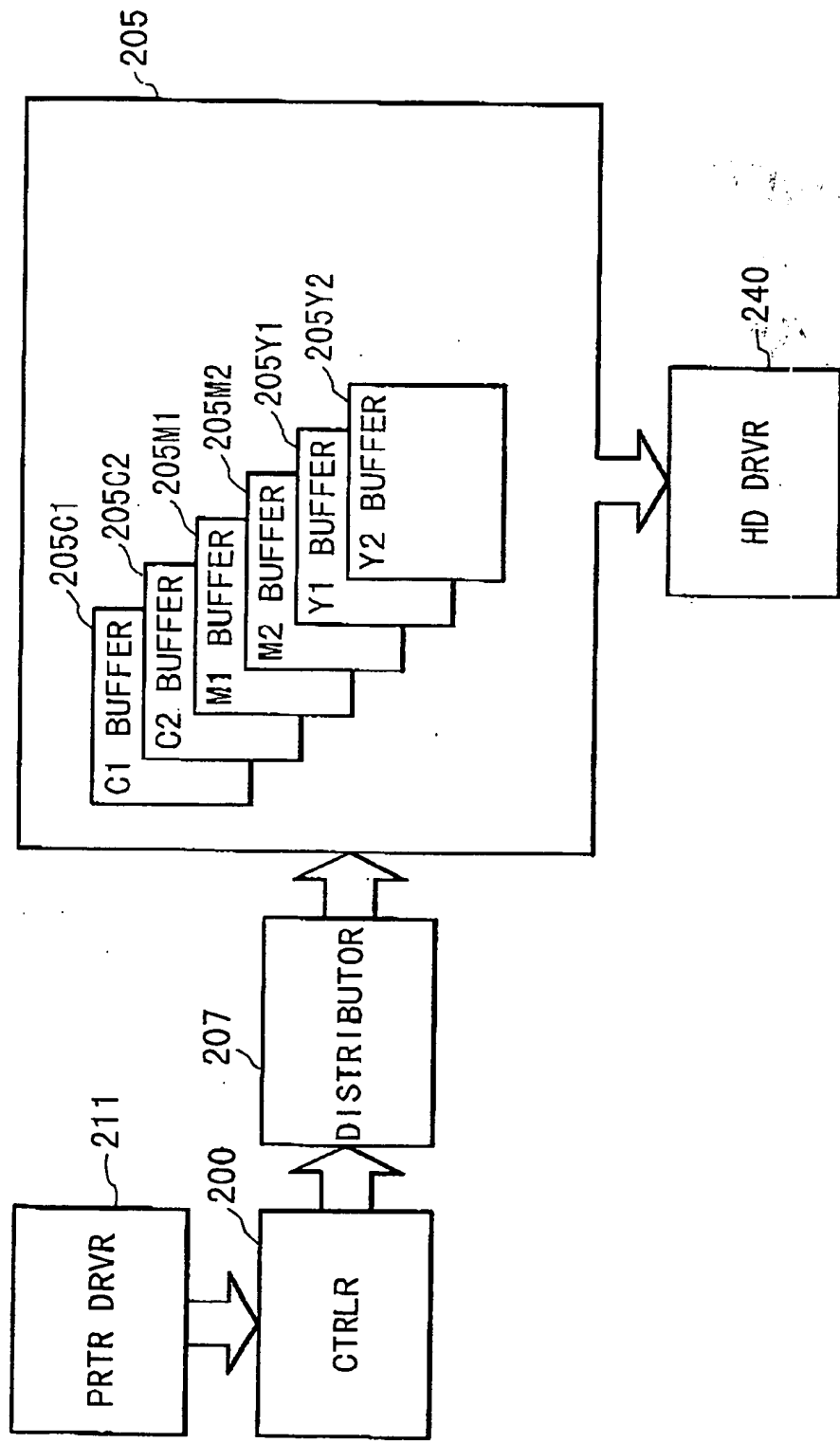


FIG. 7

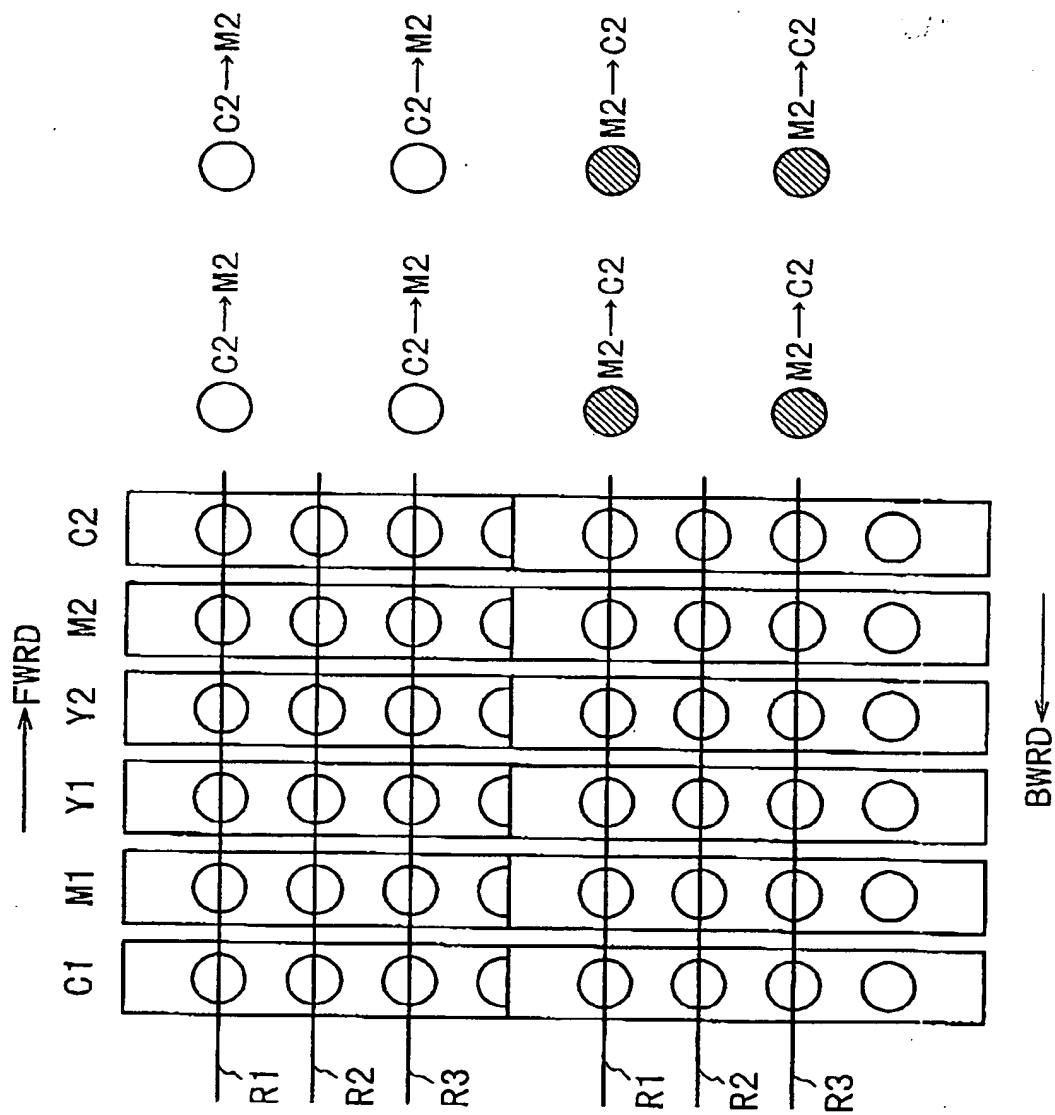
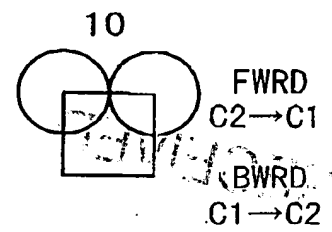
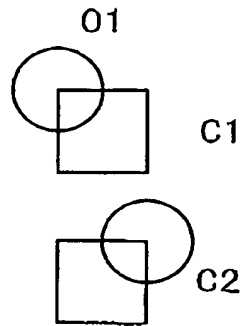


FIG. 8

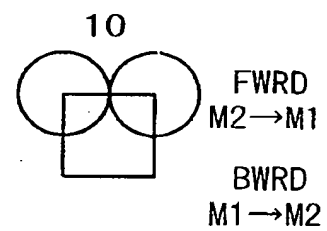
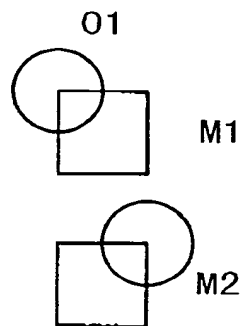
INPUT DATA 00

(a) c



INPUT DATA 00

(b) M



INPUT DATA 00

(c) Blue

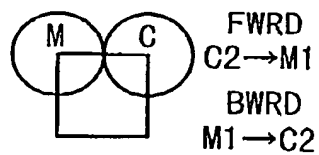
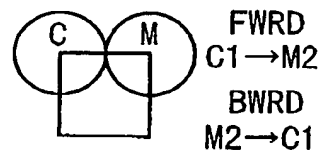
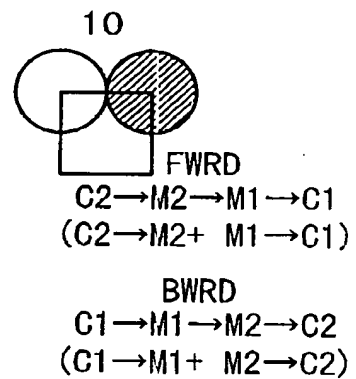
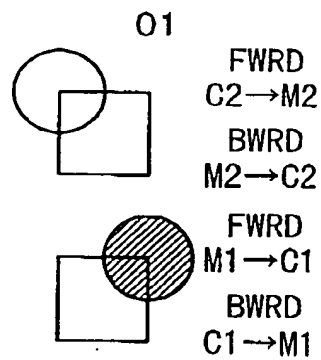
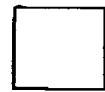


FIG. 9

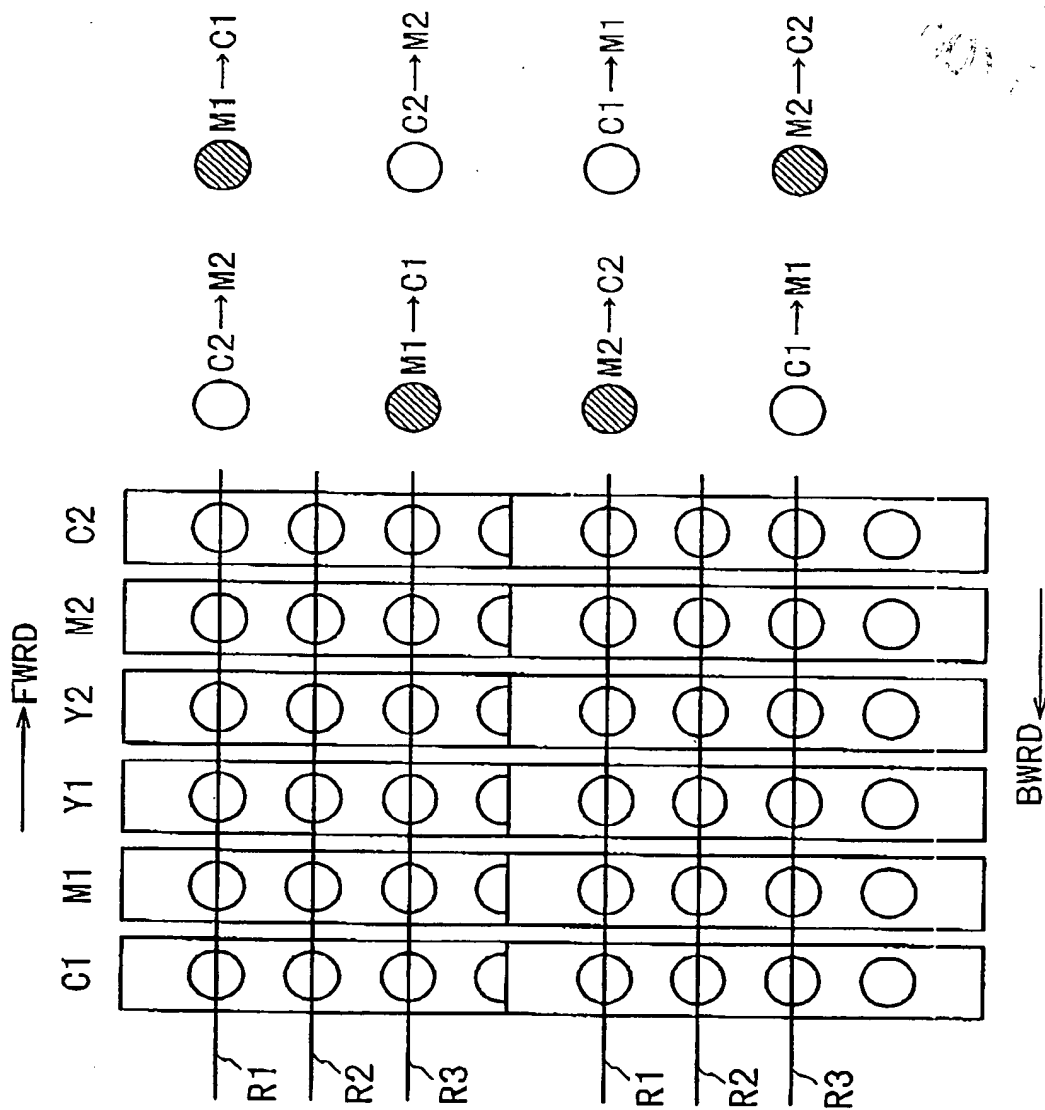


FIG. 10

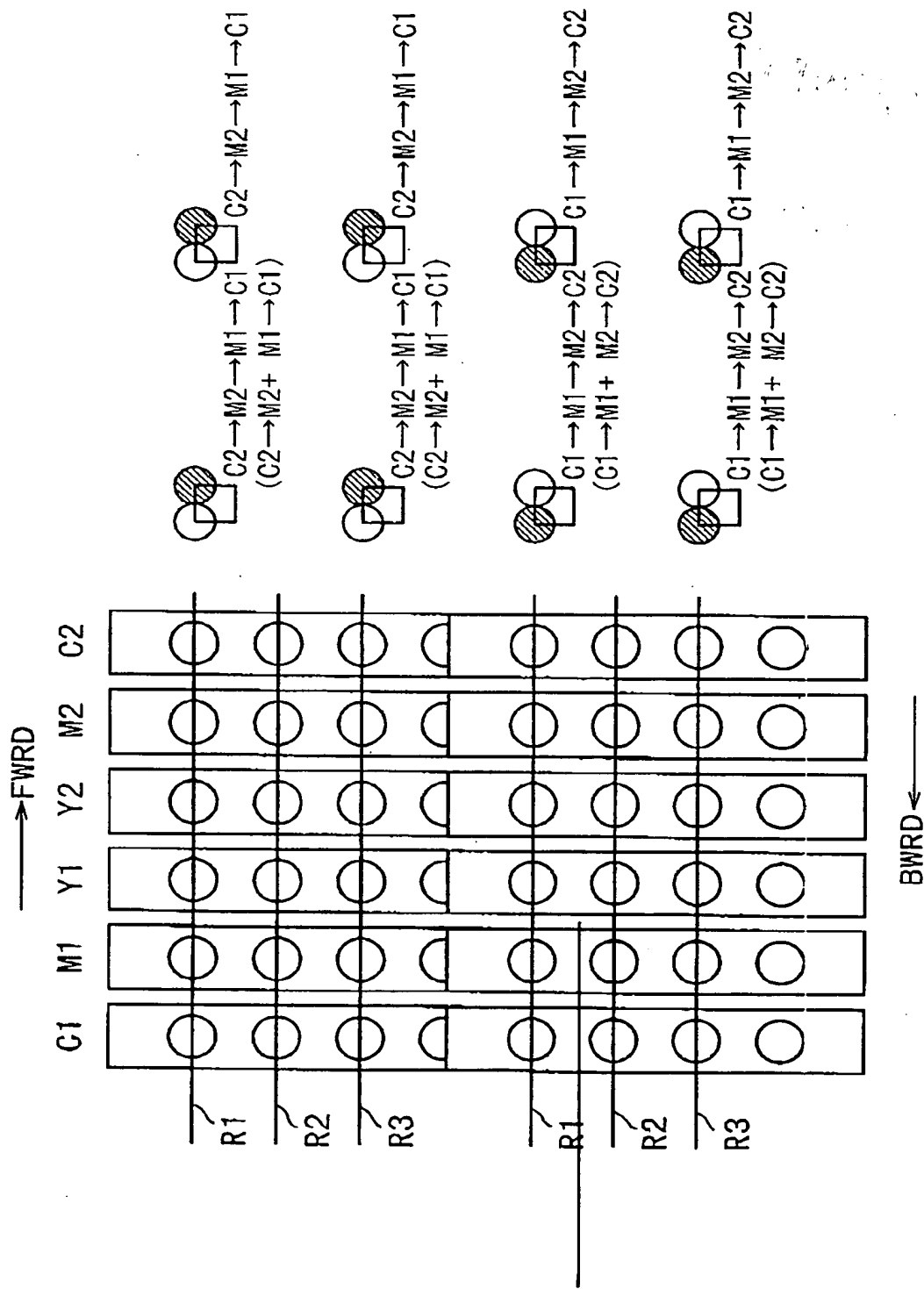


FIG. 11

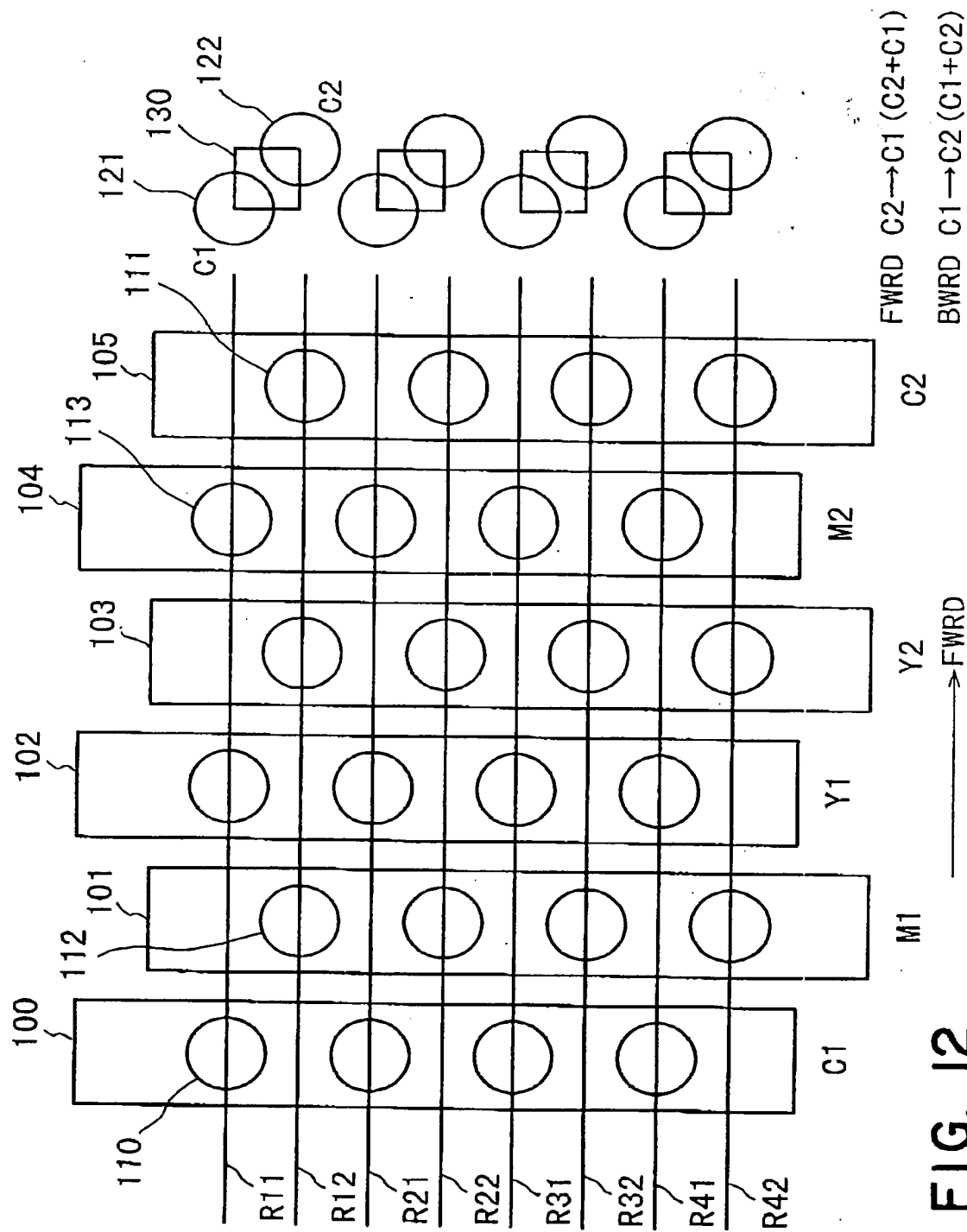


FIG. 12

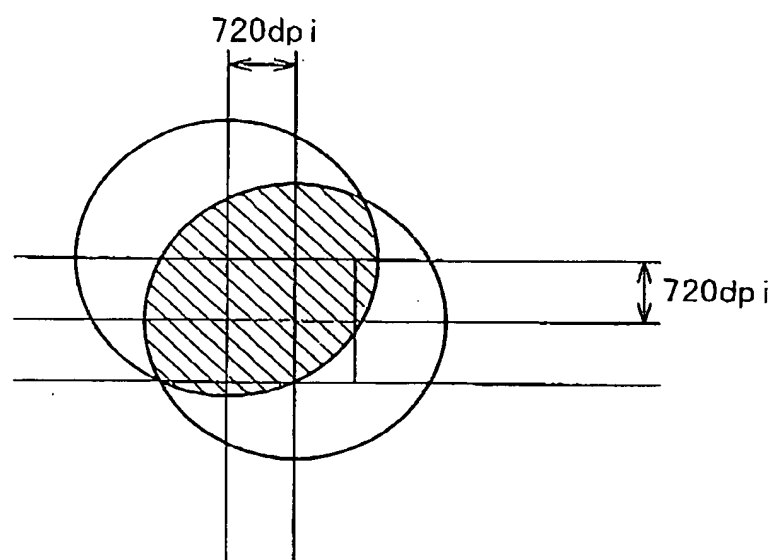
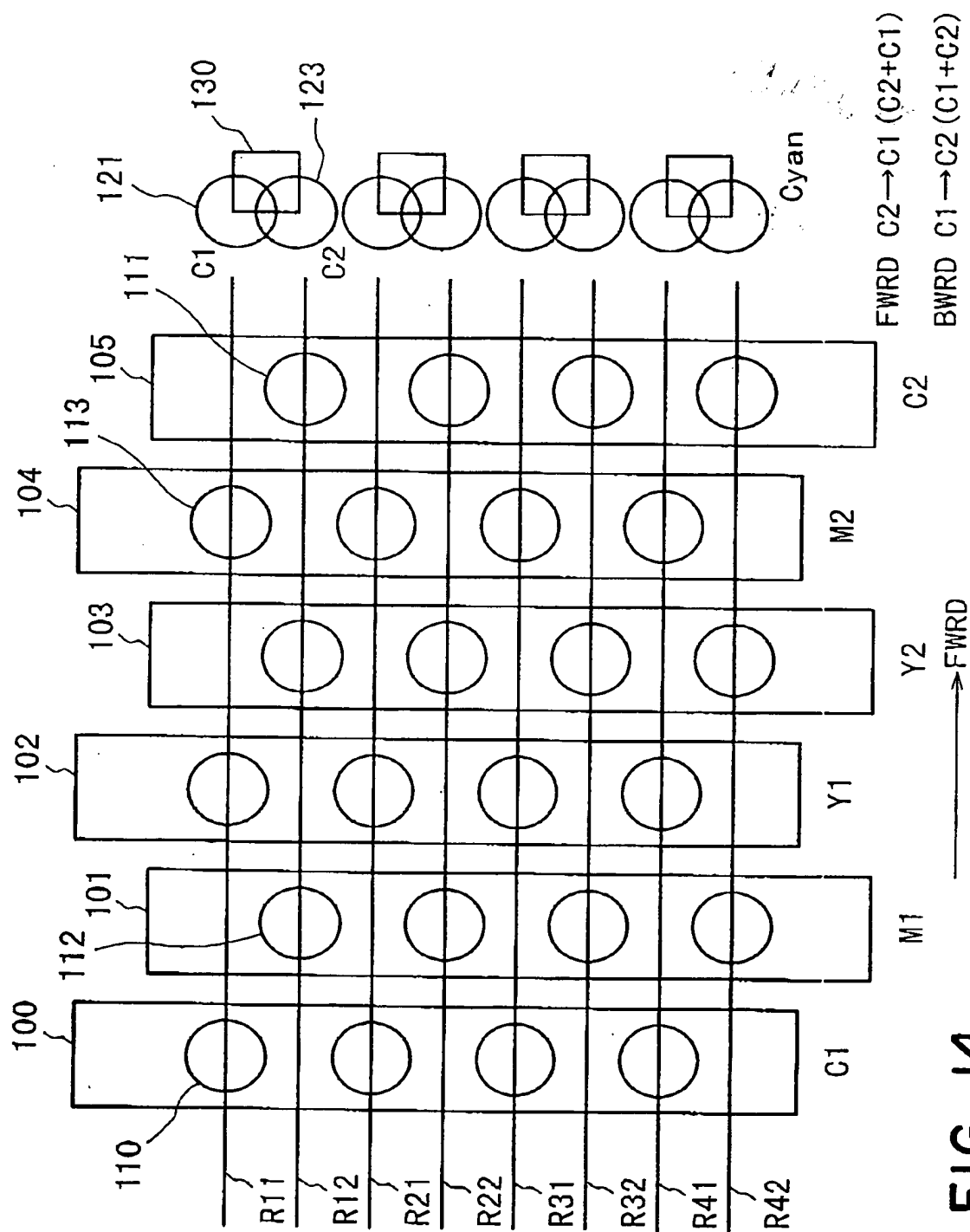


FIG. 13



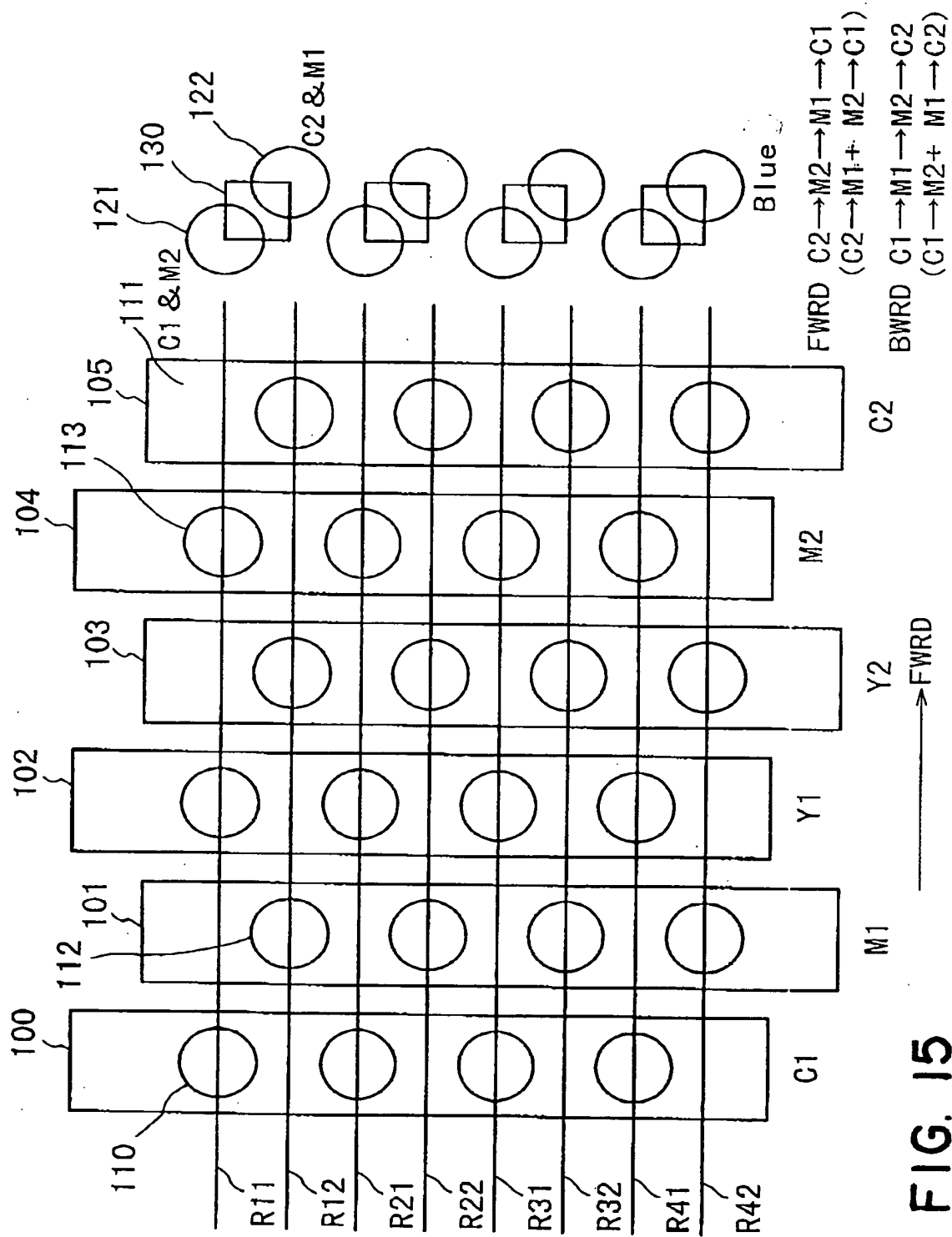
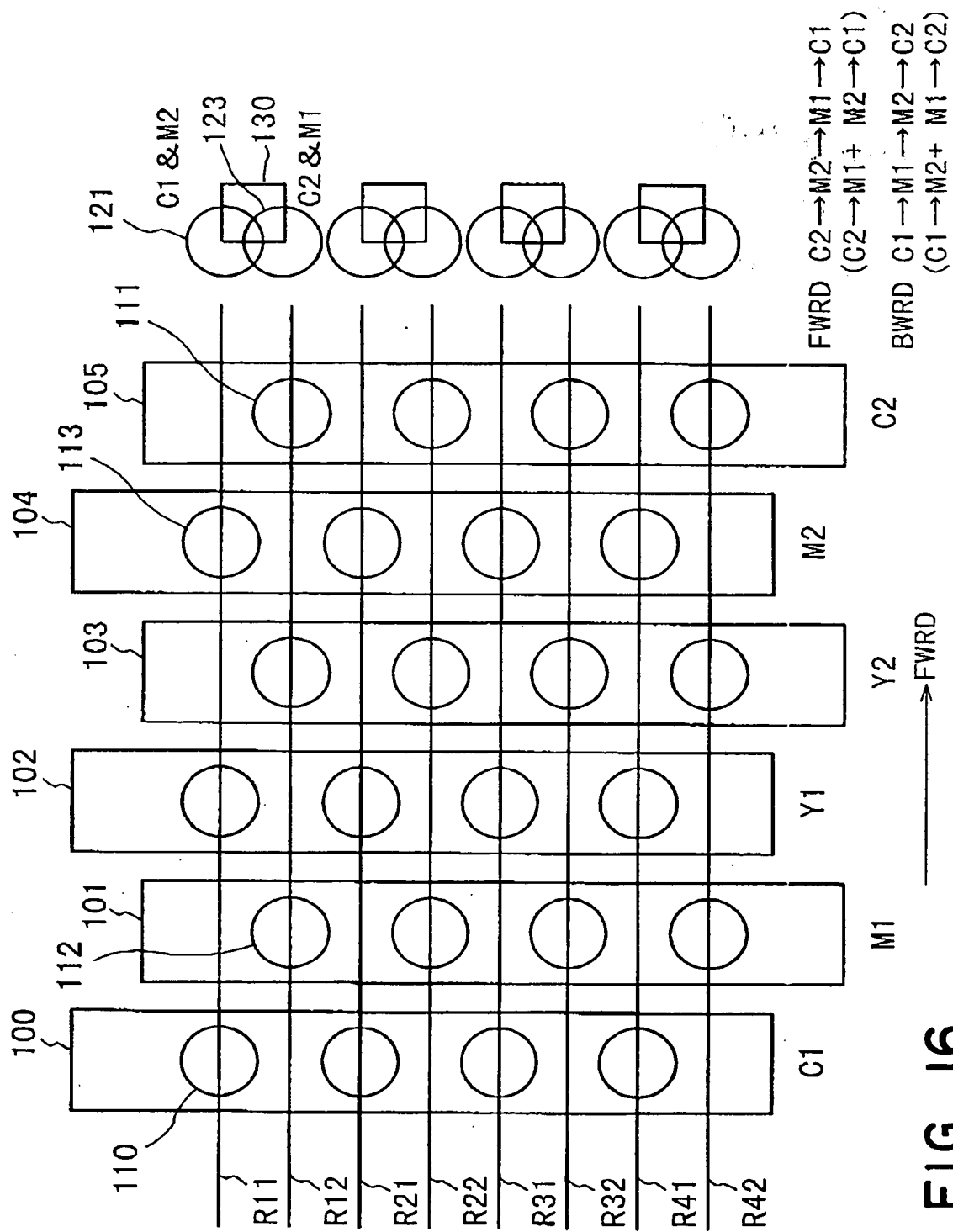


FIG. 15



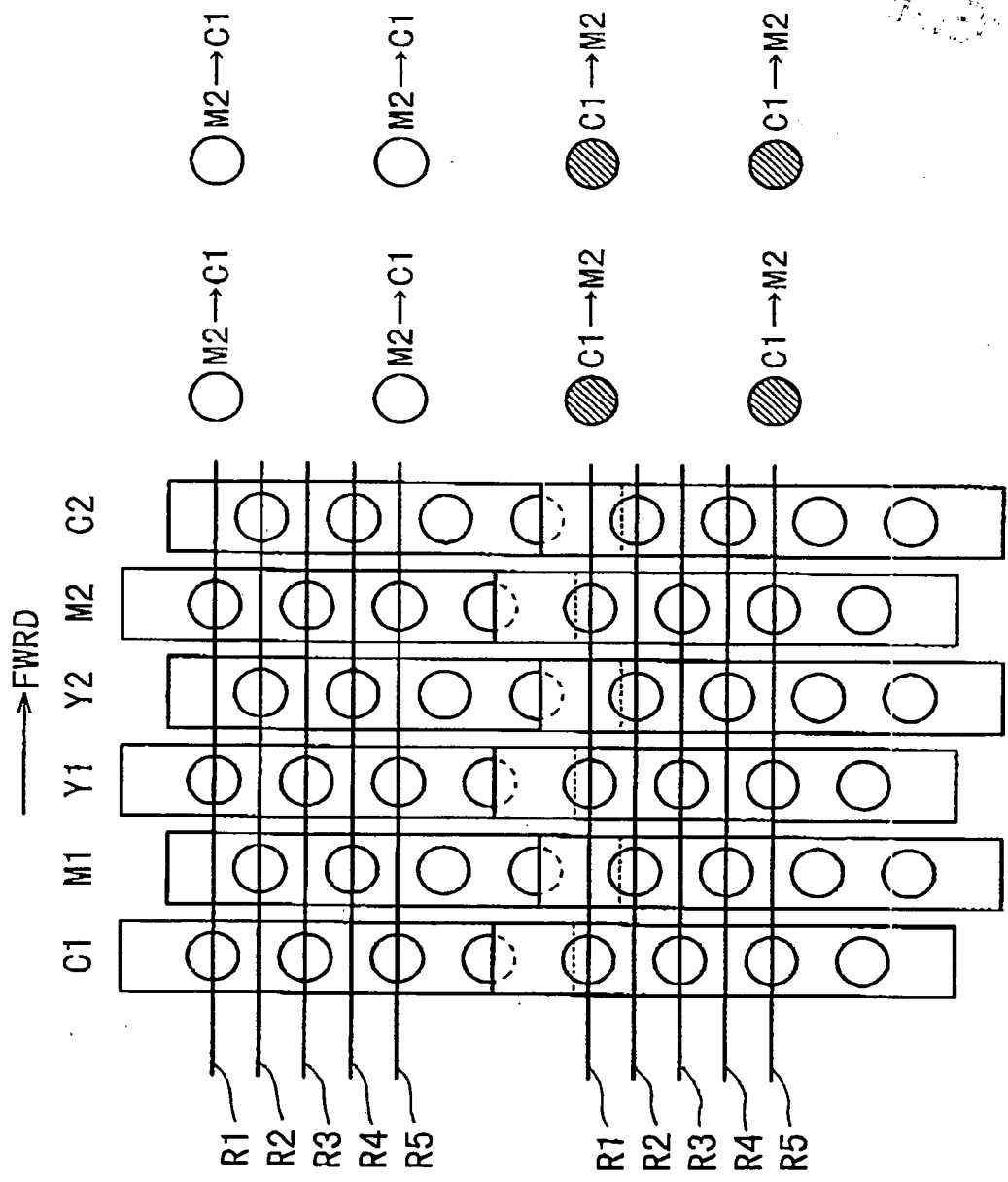


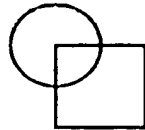
FIG. 17

INPUT DATA 00

(a) c

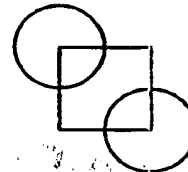


01



C1

10



FWRD
C2 → C1

BWRD
C1 → C2



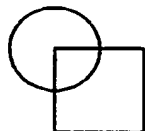
C2

INPUT DATA 00

(b) M

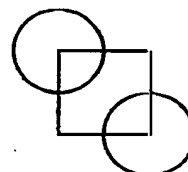


01



M2

10



FWRD
M2 → M1

BWRD
M1 → M2



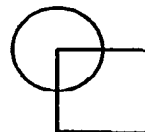
M1

INPUT DATA 00

(c) Blue



01



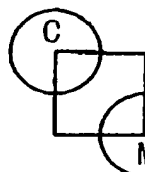
FWRD
M2 → C1

BWRD
C1 → M2



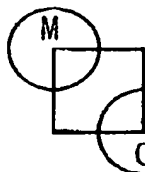
FWRD
C2 → M1

BWRD
M1 → C2



FWRD
M1 → C1

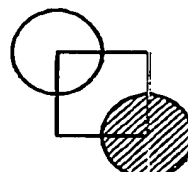
BWRD
C1 → M1



FWRD
C2 → M2

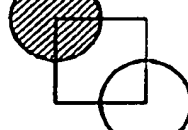
BWRD
M2 → C2

10



FWRD

C2 → M2 → M1 → C1
(C2 → M1 + M2 → C1)



BWRD

C1 → M1 → M2 → C2
(C1 → M2 + M1 → C2)

FIG. 18

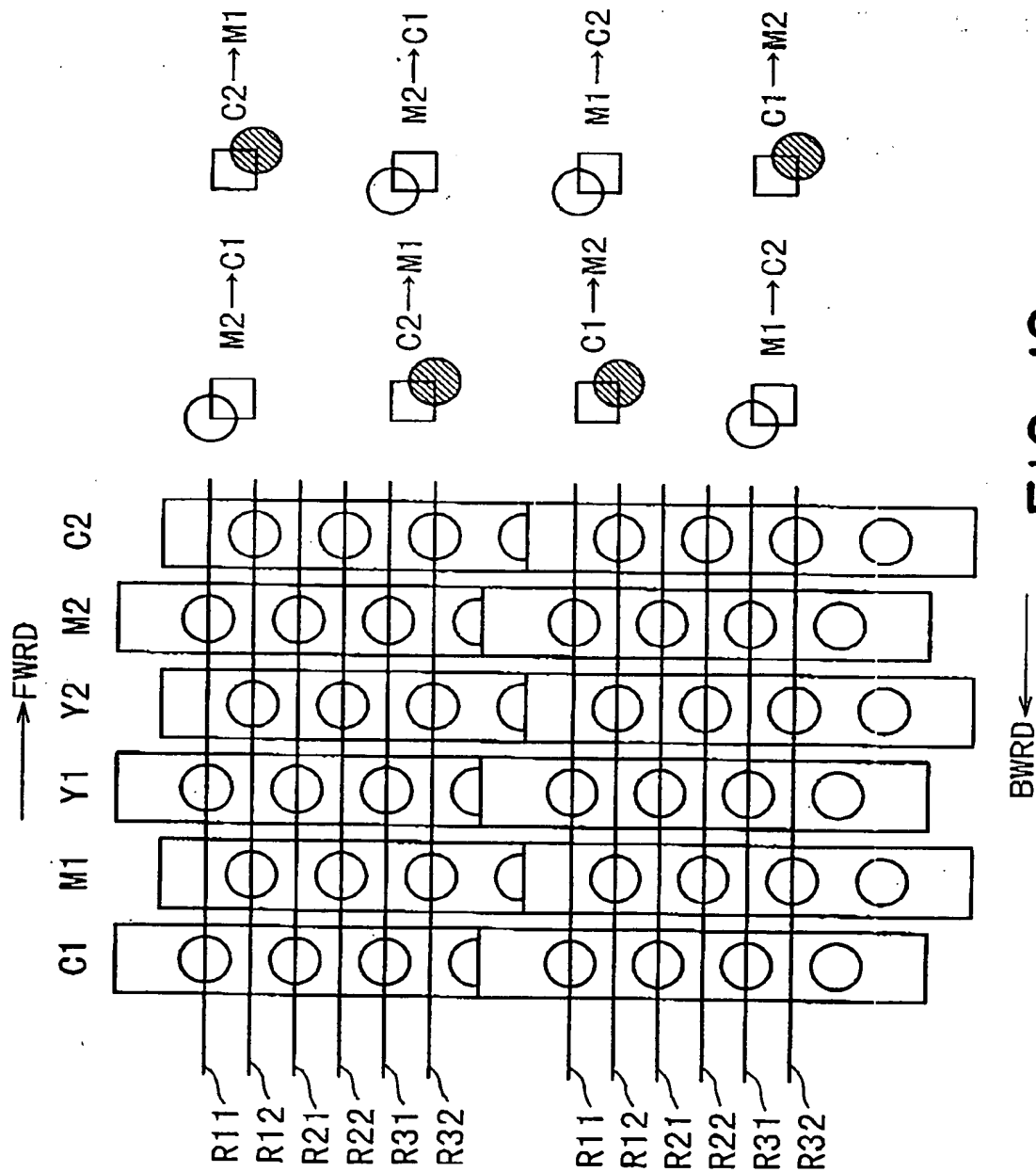


FIG. 19

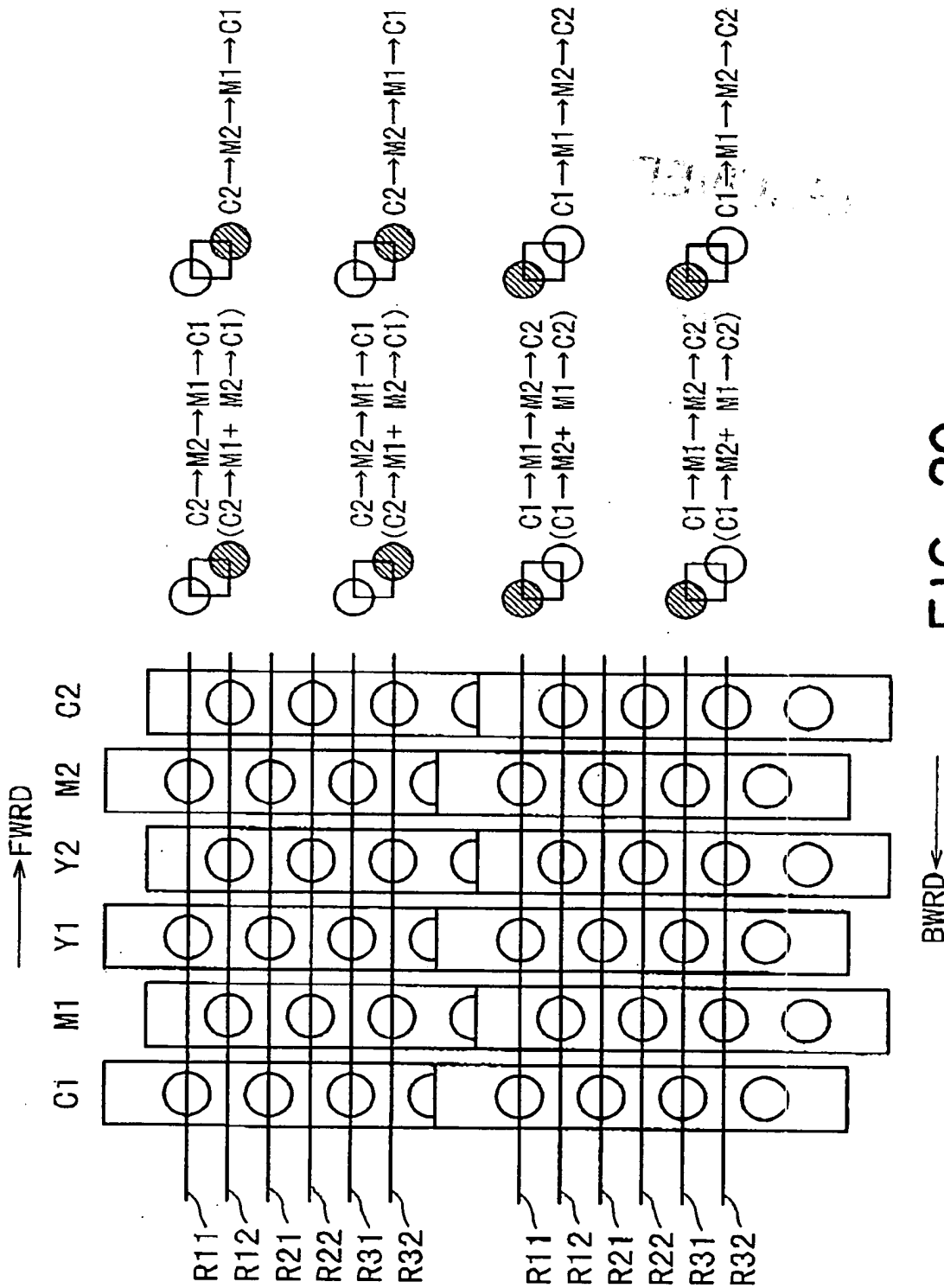


FIG. 20

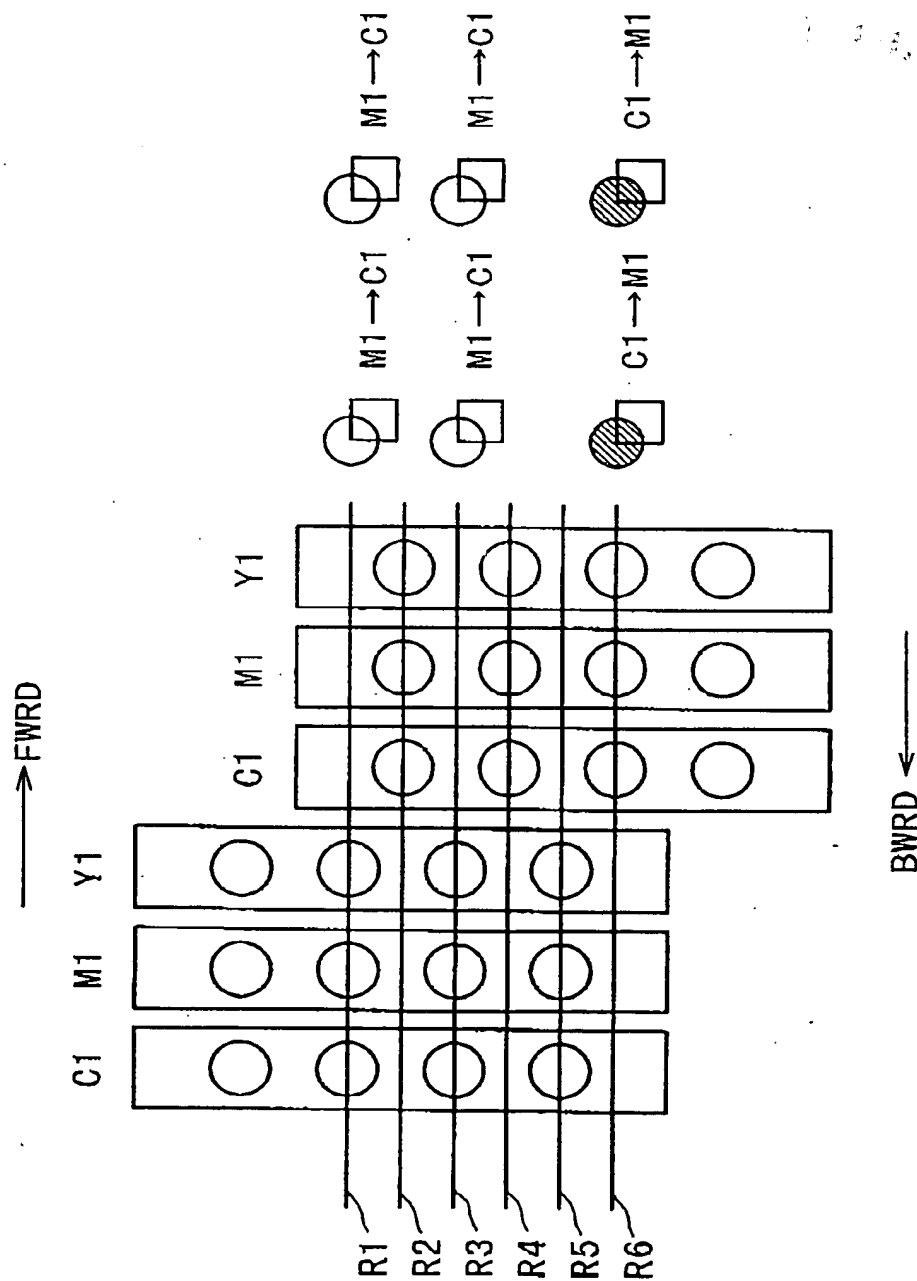


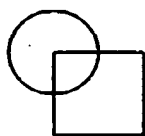
FIG. 21

INPUT DATA 00

(a) c

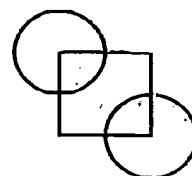


01



c1

10



$c1 \rightarrow c1$



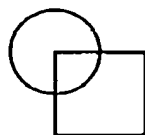
c1

INPUT DATA 00

(b) M

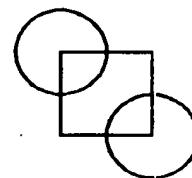


01



M1

10



$M1 \rightarrow M1$



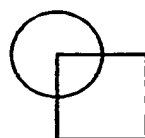
M1

INPUT DATA 00

(c) Blue

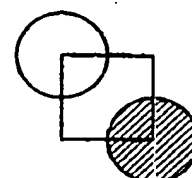


01



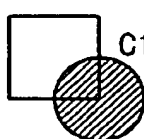
$M1 \rightarrow C1$

10



$M1 \rightarrow C1 \rightarrow C1 \rightarrow M1$
 $(M1 \rightarrow C1 + C1 \rightarrow M1)$

OR



$C1 \rightarrow M1$

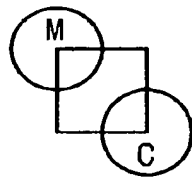
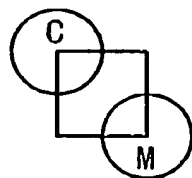


FIG. 22

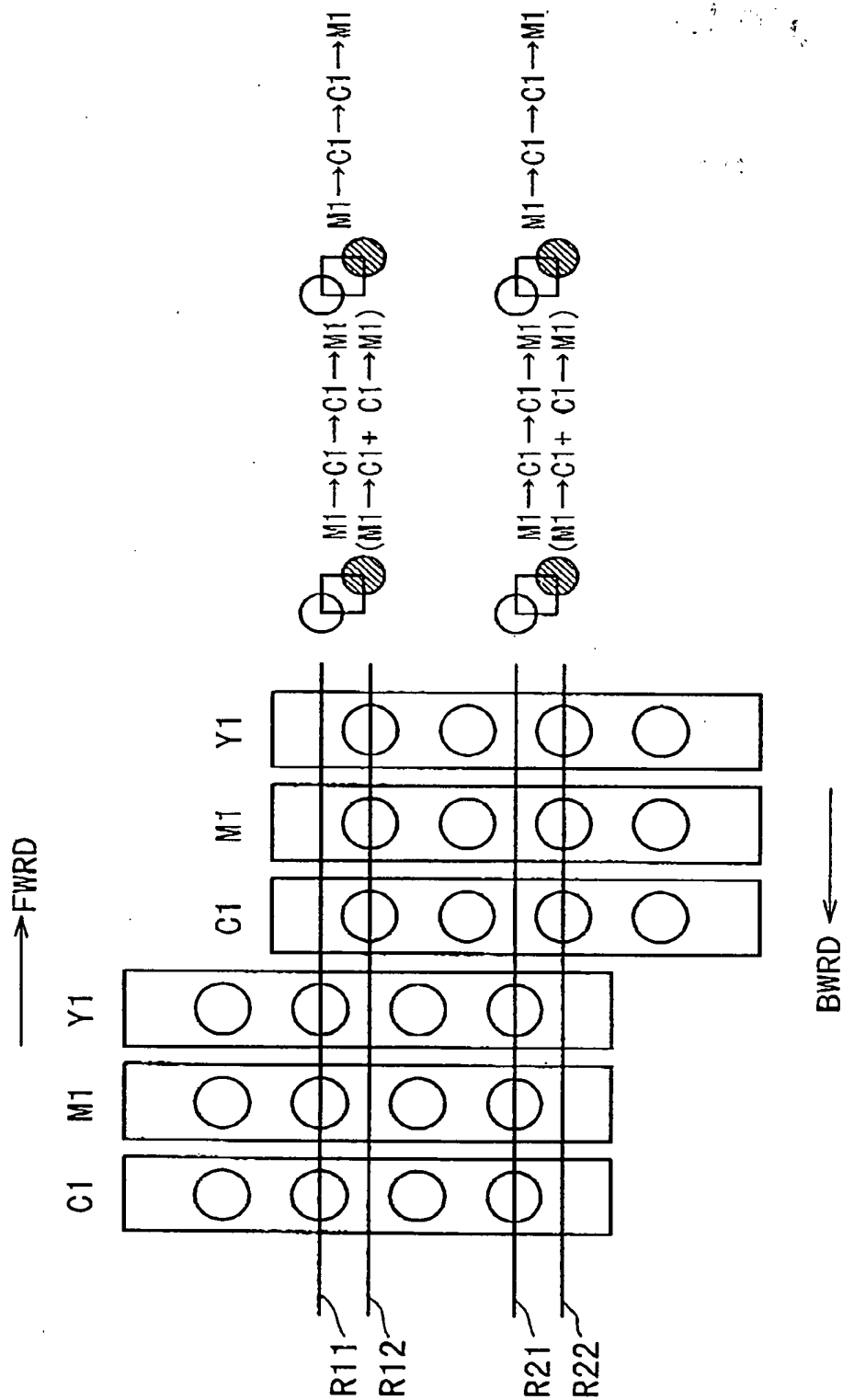


FIG. 24

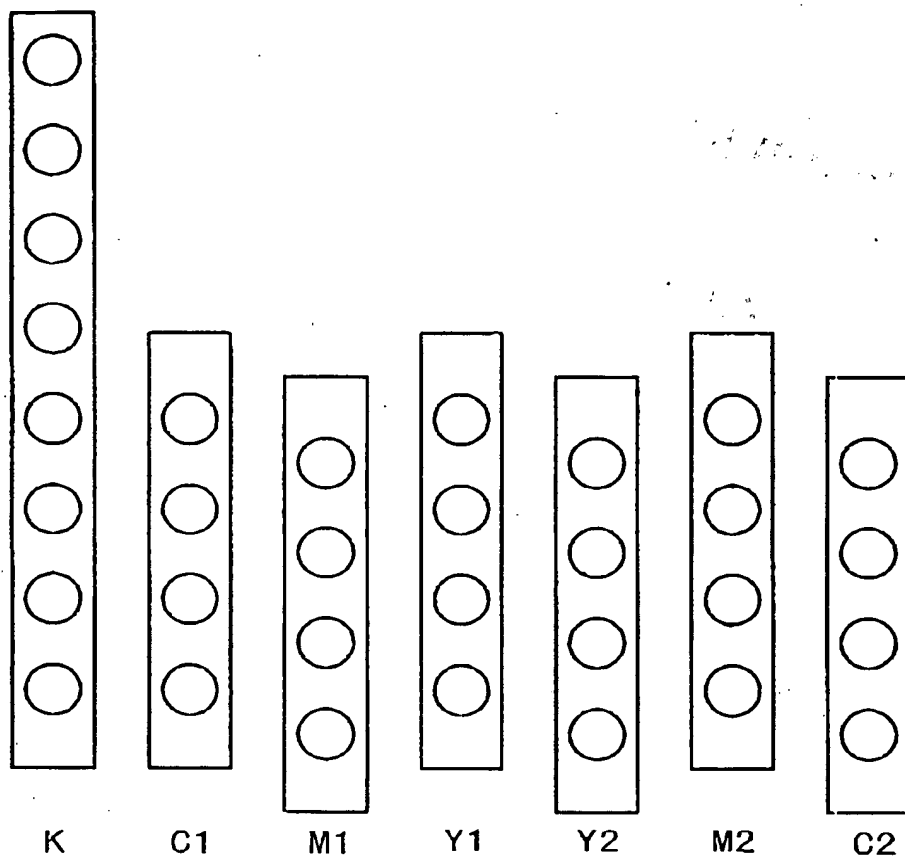


FIG. 25

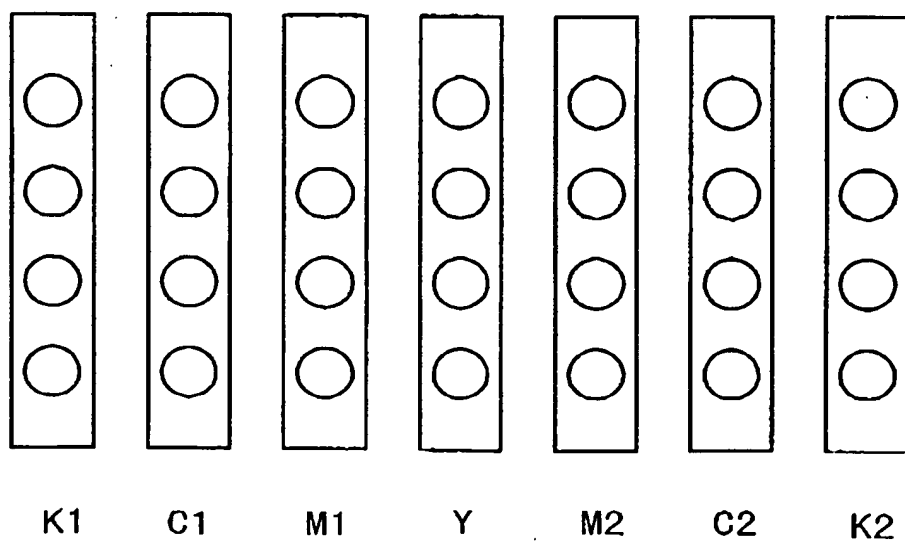


FIG. 26

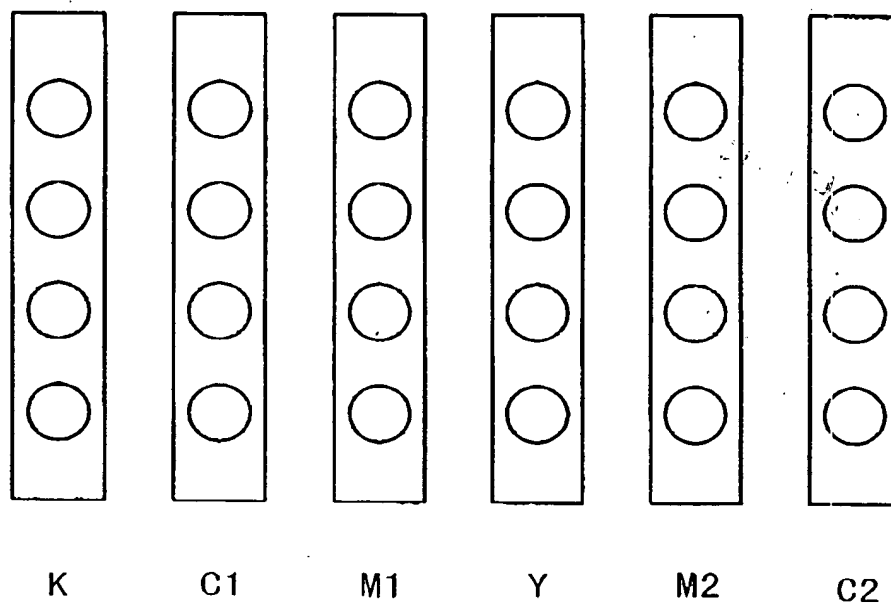


FIG. 27

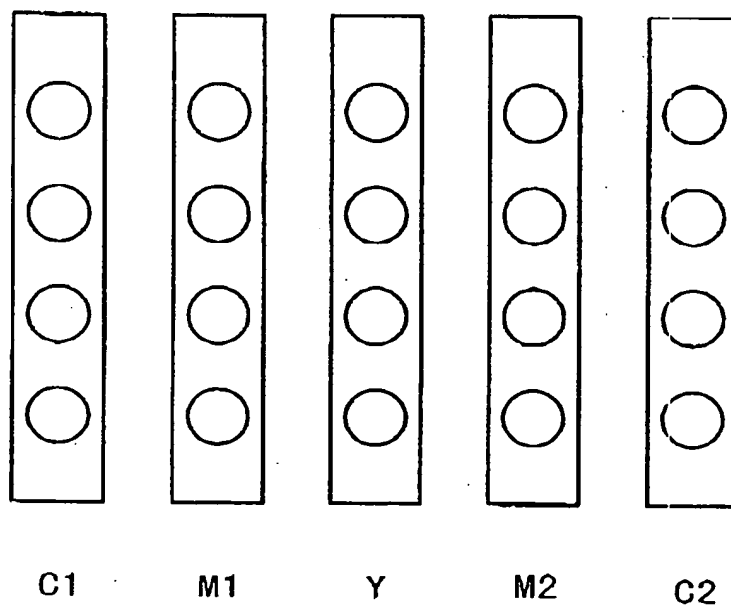


FIG. 28

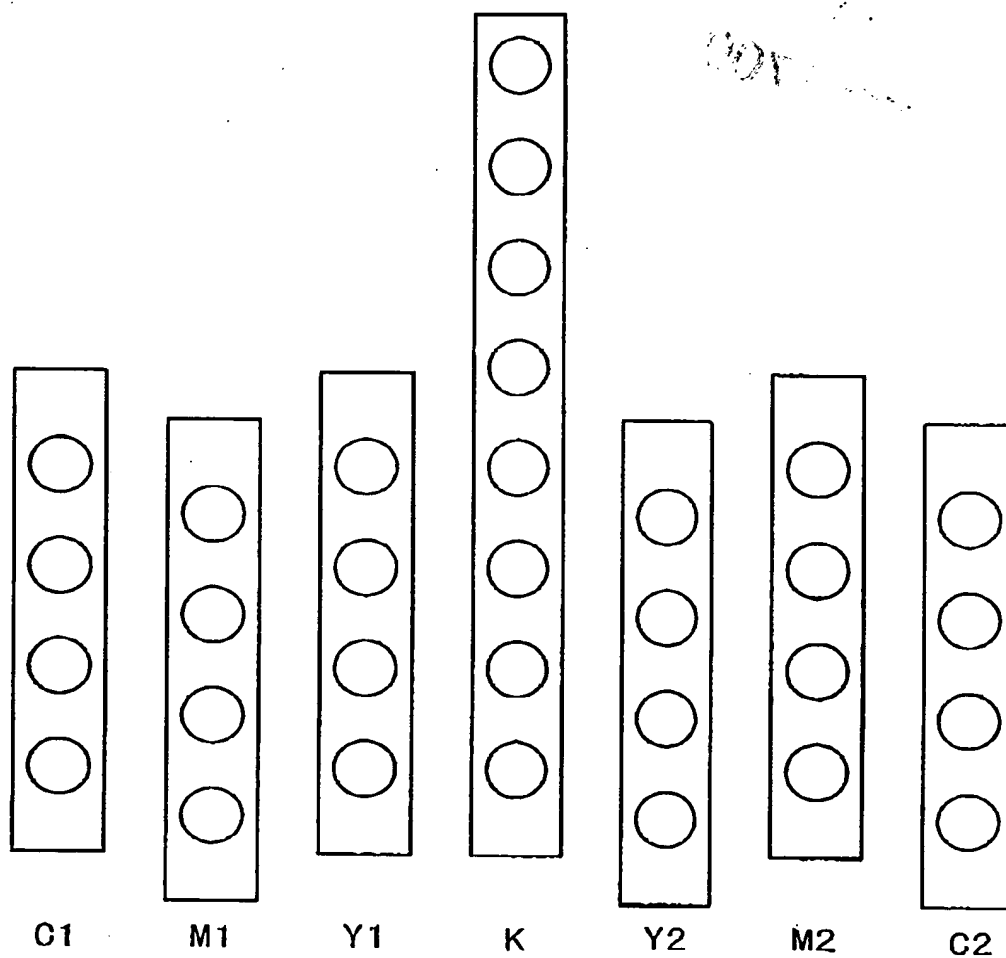


FIG. 29

